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Radiometer-on-a-chip: A path towards super-compact Submillimeter-wave imaging arrays

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ABSTRACT

A novel approach for submillimeter-wave heterodyne imaging arrays is presented in this paper. By utilizing diverse technologies such as GaAs membrane based terahertz diodes, wafer bonding, bulk Si micromachining, micro-lens optics, and CMOS 3-D chip architectures, a super-compact low-mass submillimeter-wave imaging array is envisioned. A four-wafer based silicon block for a working W-band power amplifier MMIC is demonstrated. This module drastically reduces mass and volume associated with metal block implementations without sacrificing performance. A path towards super compact array receivers in the 500-600 GHz range is described in detail.

Keywords: submillimeter imaging arrays, schottky diodes, receiver front ends

1. INTRODUCTION

Submillimeter-wave spectrometry is a proven flight technique, essential for NASA's unique goals, such as atmospheric remote sensing [1], study of cosmic water profiles [2, 3], comet characterization [4], and investigation of cosmological phenomena with radio telescopes [5]. Recently, submm technology in general and heterodyne techniques in particular have also been highlighted as an important imaging capability for both near field [6] and far field applications [7]. Most heterodyne systems being used, both for space as well as ground applications provide sufficient science data in spite of being single pixel. However, recent applications in submm have been envisioned where it becomes extremely desirable to have large format heterodyne arrays, or namely terahertz cameras. Both near field imaging, i.e. sample tomography as well as far-field imaging, i.e. threat detection can utilize array architectures to increase functionality and productivity of the technique. Similarly, while submillimeter-wave spectrometers have been flown for Earth atmospheric remote sensing as well as astrophysics missions, their use in planetary exploration has been severely restricted due to the relatively higher mass and power requirements even for single pixel systems. For in-situ submm sensors, the lack of a low-mass technology is even more exacerbating since the current state-of-the-art submm heterodyne receivers have difficulty fitting into the mass and power budgets of small platform missions.

For ground based applications, one would think, that due to relaxed mass and power constraints, heterodyne arrays would be commonplace. Unfortunately, that is not the case especially in the submm range. This is mostly due to the fact that design of heterodyne spectrometers is still focused on single pixel applications and combining several of such receivers results in a fairly massive and complicated instrument. Single pixel systems have been combined to form working array receivers either by combining them single string [8] or by using Fourier optics to use a single LO source to pump several detectors [9,10]. While both of these approaches are workable for the near-term, both will become unsustainable as pixel count is increased. Just managing the sheer mass associated with large count heterodyne arrays based on single waveguide block per chip approaches can be a challenging task.

In this paper, a technology development roadmap is presented that can drastically reduce mass and volume associated with submm heterodyne arrays. A compact semiconductor wafer stacking approach is presented that allows one to increase functionality and ultimately enable a Radiometer-on-a-chip. This approach is developed with arrays in mind and can enable heterodyne array instruments both for ground based applications as well as space exploration. Section 2

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discusses the basic concept and how this scheme can be used to decrease mass and volume and increase pixel count. Section 3 discusses preliminary results that have been obtained by packaging a W-band power amplifier chip validating this approach for submm work. A summary is presented in Section 4.

2. RADIOMETER-ON-A-CHIP

2.1 Basic Concept

A functional block diagram of a heterodyne receiver and a picture of an existing submm receiver front-end (RFE) is shown in Figure 1. This RFE is based on taking an input signal around 18 GHz, multiplying it by a sextupler and amplifying it with the help of a power amplifier module. The amplified signal is then used to drive the submm tripler which in turn then pumps a sub-harmonic mixer. This particular receiver covers the 530-590 GHz range, is around 800 grams and occupies a $20 \times 3 \times 3$ cm³ space. Detailed results from this mixer have been presented elsewhere [11]. It is instructive to delve a little deeper into each component of this RFE. The active multiplier is based on a x2 active multiplier chip followed by a MMIC amplifier chip. This is followed by a passive x3 circuit all in the same block. The power amplifier module is based, in this particular instance, on a set of five pHEMT based power amplifier MMICs. The submm tripler has been discussed in detail in [12] and is based on the GaAs Schottky diode process that provides chips on very thin membranes. The mixer is also based on a GaAs membrane Schottky process.

Instead of packaging one chip at a time the idea is to demonstrate that wafers can be “bonded” together to provide a robust, extremely powerful way of making submm receivers with vertically integrated functionality. Based on the recent advances in semiconductor circuit designs and manufacturing it is now possible to envision a complete submm radiometer-on-a-chip. The concept that will be validated is conceptually shown in Figure 2. A stack of 8 different “wafers” is bonded to provide functionality of a receiver all in a package that is approximately 0.3 cubic centimeters. This represents a drastic reduction of mass and volume from the current state-of-the-art.

The base layer of this arrangement could be a duroid board or a highly integrated 3-D CMOS chip that provides Command, Data and Handling capability along with a low-noise amplifier in the IF band. The second wafer in the stack provides VCO capability and is controlled by the base layer wafer. Based on the application at hand an appropriate VCO technology can be selected for this wafer. It is envisioned that the VCO functionality will be around Ka-band though as VCO technology progresses this wafer could provide input at much higher frequencies. The next wafer in the scheme will multiply the Ka-band signal from the VCO to a W-band signal. This will be achieved by a combination of Ka-band power amps and active multiplication. The signal interface between the two wafers would be similar to the vertical co-axial discussed in [13]. However, the interface for passing the W-band signal between the active multiplier wafer and the power amp at W-band would probably have to be different from the co-axial architecture. We have investigated the use of ‘waveguides’ for this interface and will discuss recent results later in this paper. The W-band power amplifier wafer will appropriately amplify the signal so that it can be used to drive the tripler MMIC that in turn will pump the subharmonically pumped mixer MMIC. Wafer 5 provides the waveguide interface between wafers 4 and 6 and can be machined from silicon. Wafer 6 will be a wafer based on the submm schottky diode technology that allows for low parasitic schottky diode circuits. Finally, to couple the RF signal a broadband antenna technology that is consistent with semiconductor fabrication technology is envisioned. Wafers 7 and 8 are dedicated to achieving this functionality. Further details on the antenna structure are provided later. By integrating at the wafer level, customizing the interconnects and planarizing the transmission media a super compact RFE can be achieved.

2.2 Implementation approach

While ultimately it will be possible to integrate the various wafers via advanced wafer bonding technology, a simpler implementation approach has been adopted for preliminary validation. In this approach, commonly available silicon wafers are used as “host wafers” and the chips mentioned above are packaged in them. A fundamental issue that needs to be resolved for this implementation is how to transmit the signal between the different wafers, especially as the operating frequency is increased. We have developed a process of making this interconnect via a vertical waveguide structure which is especially useful for the submm range.

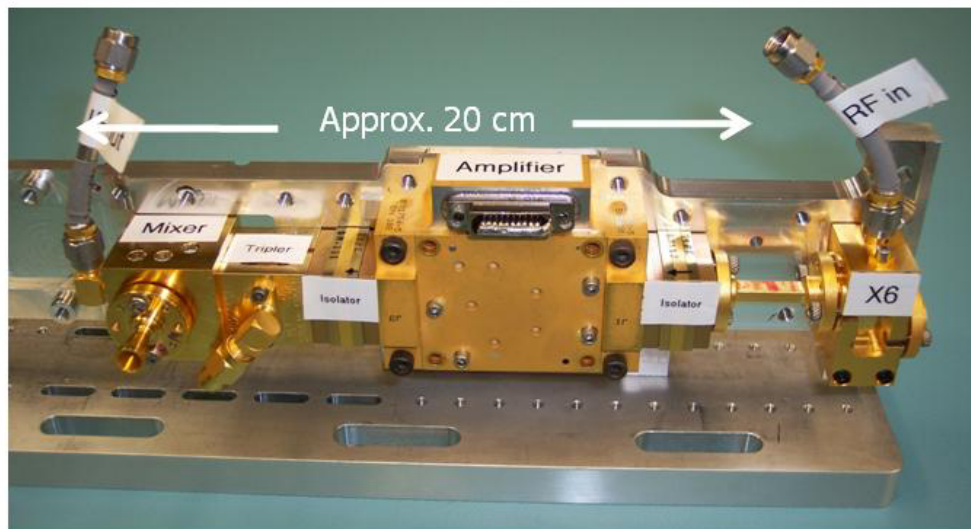
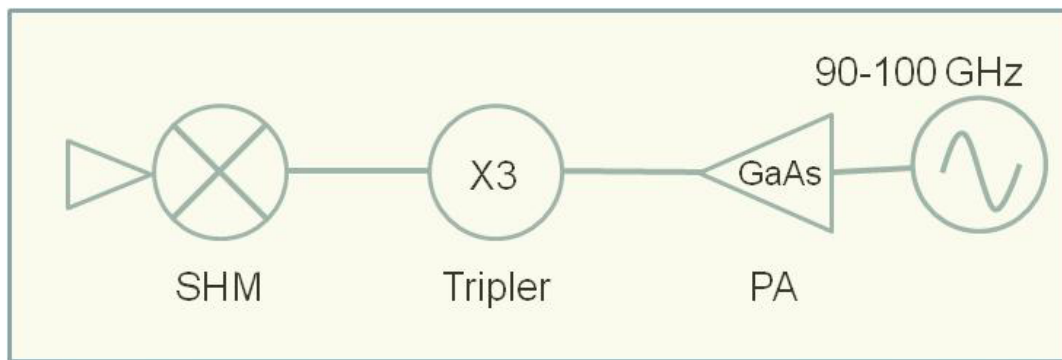


Figure 1: A functional block diagram of a heterodyne receiver front-end is shown in the top. A prototype RFE in the 500-600 GHz range is shown below.

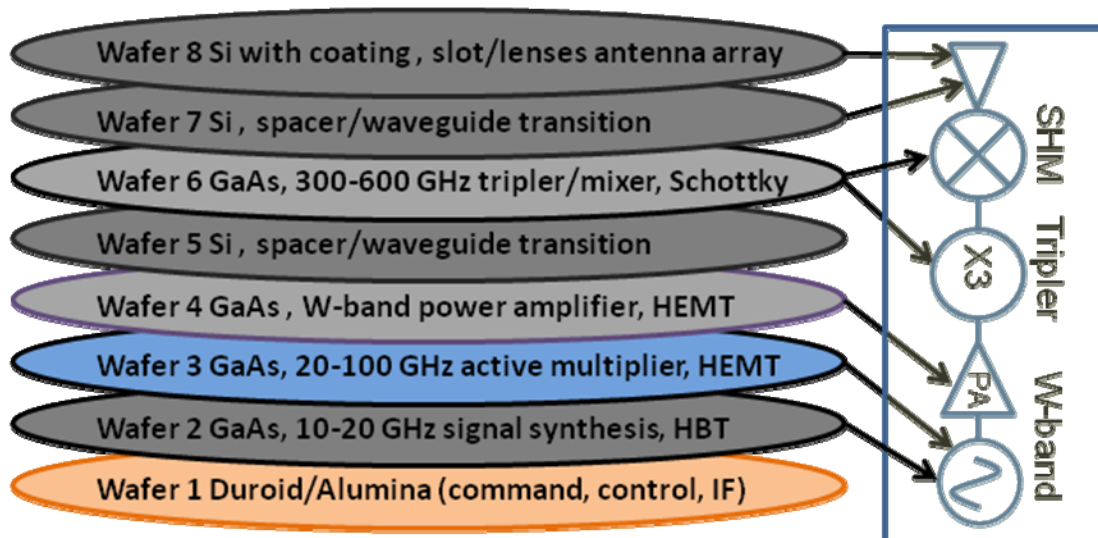


Figure 2: A proposed 8 wafer scheme that can result in super compact heterodyne receiver arrays. A functional block diagram is shown at the right.

Silicon micromachining has been used to make waveguide structures and circuits as reported in various references[14,15]. However, all of these methods involve splitting the silicon block in the E-plane and assembling the two pieces of silicon to form the circuit. To interface with this silicon block, however, the metal waveguide needs to ‘mate’ well with edge of the assembled block. Photonic structures to reduce losses have been suggested but these require additional processing steps further complicated by the fact that they need to be made on the edge of the silicon wafer. This scheme has a number of issues, especially as operating frequency is increased. The surface roughness on the edge of the silicon is difficult to control and similarly the vertical edge profile is often less than perfect. Both of these artifacts can drastically increase losses, especially at higher frequencies. In our scheme we have utilized the plane surface of the silicon to make the silicon-metal interface. This is explained in Figure 3. The traditional approach is shown on the left while the “vertical waveguide” approach is shown on the right. The waveguide circuit is still split at the E-plane so a transition is required to turn the input waveguide by 90 degrees. A multi-steps bend can be utilized to accomplish this [16]. Simulation results confirm that even with a single step one can obtain a broadband interface to the metallic waveguide.

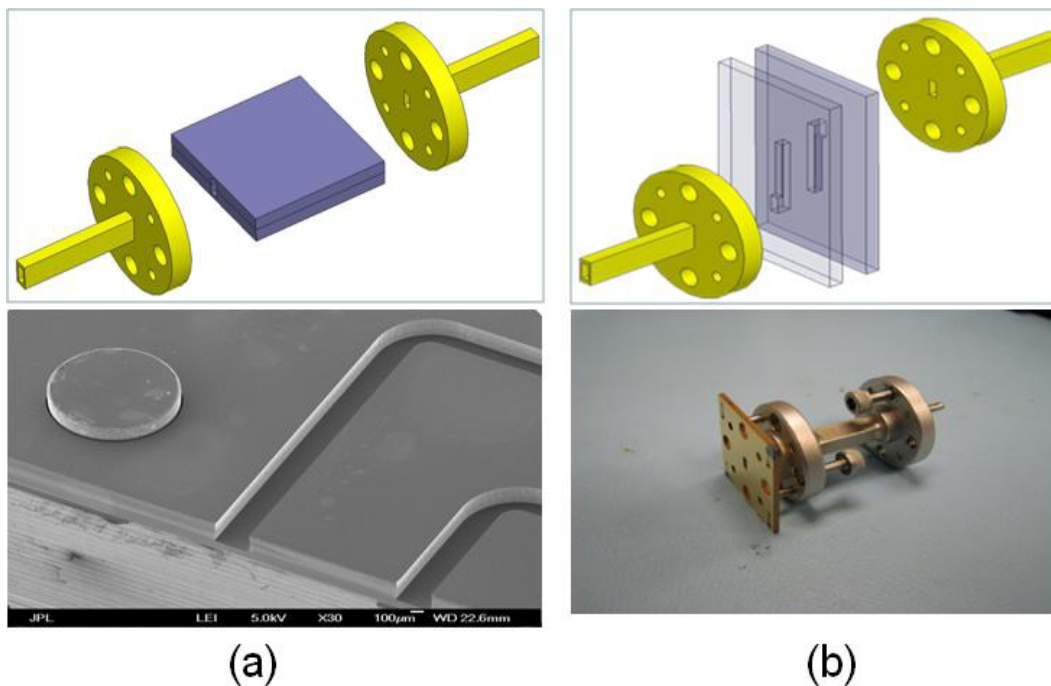


Figure 3: Two approaches for defining Si to metal interface are highlighted in this figure. The traditional concept of splitting the waveguide block at the E-plane and making contact to the edge of the Si block is shown in (a). The method used here is shown in (b). The plane surface of the silicon is used to interface with the metallic waveguide. This contact is now robust, reproducible and independent of the silicon etch quality.

2.3 Submm Array receivers

Submm or THz imaging has become a topic of great interest recently due to its use for concealed weapons detection. A recent survey of this field has been presented in [17]. Passive thermal imaging in the 100-300 GHz range is the most mature technology, with several companies now offering complete near-video rate imaging systems [18]. Drawbacks of the passive detection approach include an unfavorable tradeoff between threat contrast and image resolution at frequencies exceeding 100 GHz; problems with signal clutter from uncontrolled environmental illumination conditions; and weak contrast from objects concealed by multiple layers of clothing.

These drawbacks can be overcome by using active imagers at higher frequencies, but commercialization of such systems has been slow, in part because of the significant problem of clutter and speckle in detecting the reflection of coherent radiation from complex targets such as clothed persons. In 2008, however, JPL demonstrated a breakthrough radar-based approach to active THz imaging that overcomes the clutter problem using conventional single pixel heterodyne detection electronics [19]. Subsequently, activity in THz radar imaging has picked up, but so far JPL has the unique ability to generate rapid, high resolution radar images at standoff ranges up to 25 meters.

JPL's THz imager uses the frequency modulated, continuous wave (FMCW) radar technique with a 30 GHz bandwidth spanning the range 660 to 690 GHz. However, only single pixel architecture has been demonstrated thus far. The system along with some images is shown in Figure 4. The current imaging time for a $20 \times 20 \text{ cm}^2$ area at a distance of $\sim 25 \text{ m}$ is 3 seconds. This relies on moving a scanning mirror with a superfast motor (motor acceleration of $16,000 \text{ degrees/sec}^2$). With the same setup, imaging speed can be increased by a factor of 10 by going to a linear array of 1×8 .

The approach proposed in this paper is ideally suited for building array receivers. Since wafer level integration is proposed building a multi-pixel receiver should cost no more than building a single pixel receiver as far as the receiver front end electronics are concerned. An important roadblock for building array receivers also lies in the antenna structure that can be used with a large system. To overcome this bottleneck a micro-lens antenna has been proposed, which can be fabricated photo-lithographically, as shown in Figure 5 [20]. The antenna geometry consists of a waveguide feed that excites a silicon lens antenna through a leaky-wave or Fabry-Perot resonant cavity. This cavity is used to match the waveguide feed with the silicon medium as well as to illuminate the upper part of the lens. Thanks to this illumination, the lens sector can be fabricated with photo-lithographic techniques.

The feed is a square waveguide propagating the TE_{10} mode. This waveguide is loaded with a double slot iris. The iris is used for matching the antenna and for suppressing undesired modes that can propagate in the cavity. The description of the geometrical parameters of the feed is shown in Fig.5b. Between the waveguide feed and the dielectric lens, ϵ_r , there is a cavity of dimension h and dielectric constant ϵ_{rc} . A couple of TE/TM leaky waves poles pointing towards broadside will be excited when $\epsilon_{rc} < \epsilon_r$ and $h \approx 0.5 \lambda_0 / \sqrt{\epsilon_{rc}}$. On top of the cavity, we placed an extended hemispherical lens defined with the extension height L and the radius R . Only a small sector (θ_s) of the lens is actually used. A calculated electric field distribution for such a micro-lens is shown in Figure 5(c). Measured beam patterns conform to theory and have been measured up to 600 GHz [21].

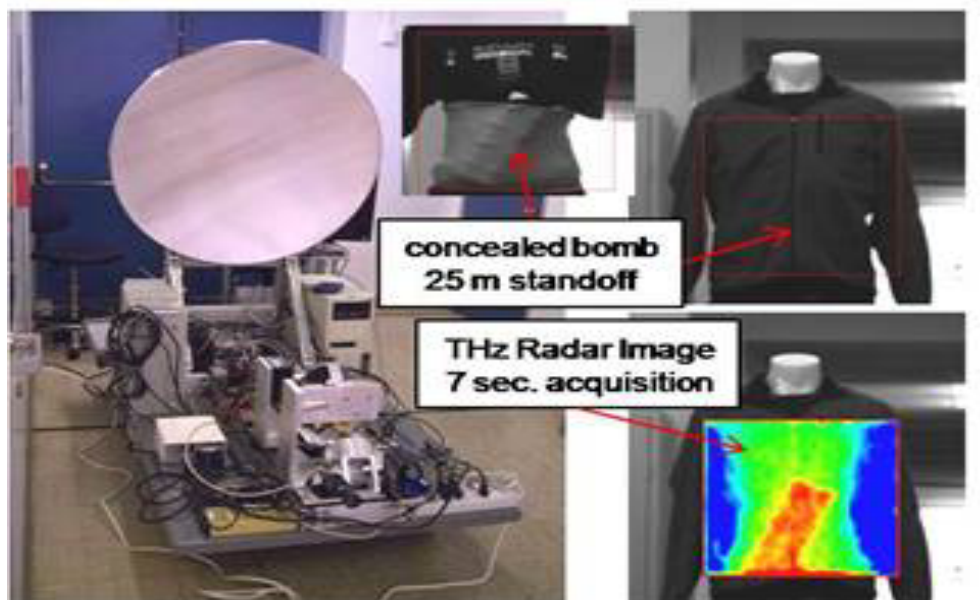


Figure 4: The prototype JPL active submm concealed weapons imager is shown on the left. Images obtained at 25m standoff requiring 7 seconds are shown.

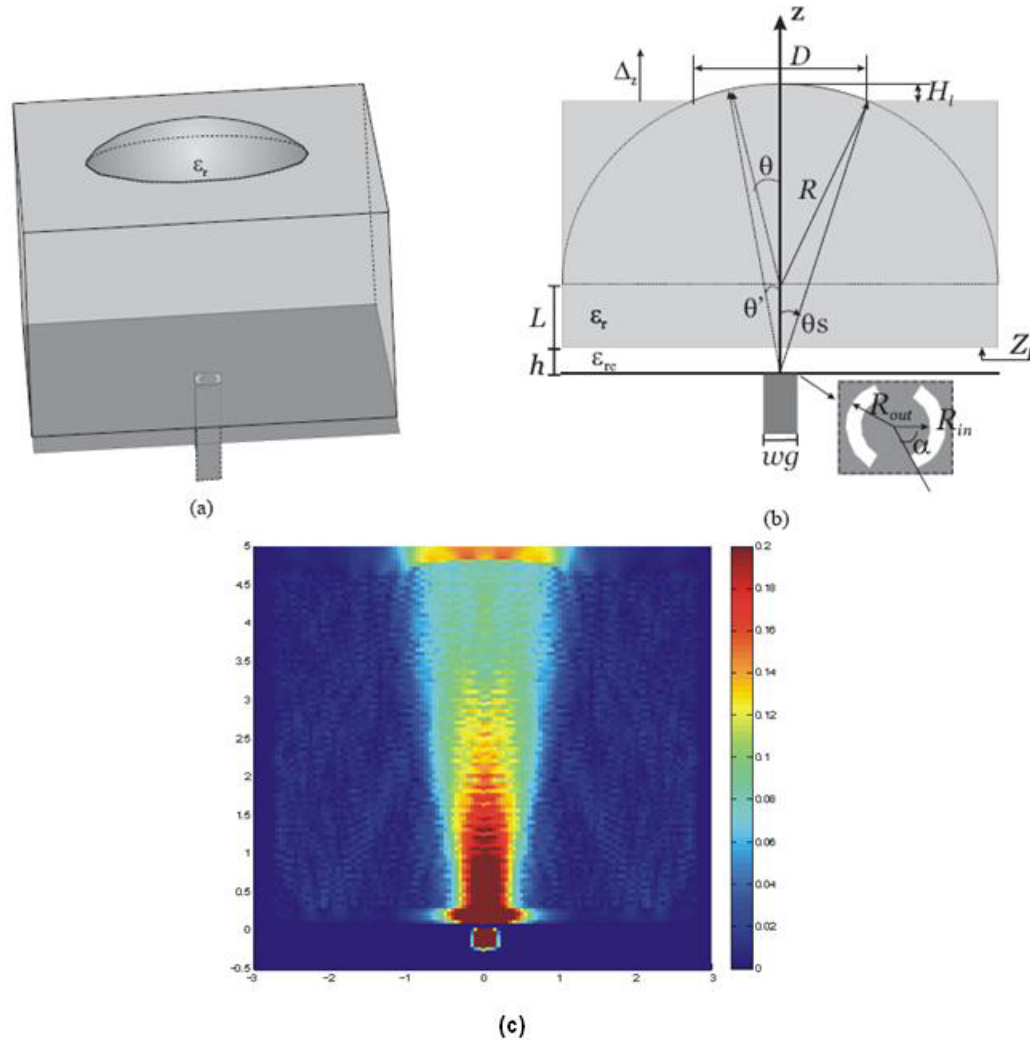


Figure 5: Micro-lens antenna that is consistent with micro-fabrication technology. (a) 3-D view, (b) side view, (c) simulated electric field distribution for the micro-lens.

3. RESULTS

The implementation approach described above has been used for several components. A power amplifier chip has been packaged in a stack of four Silicon wafers. This is discussed in Figure 6. The top two pieces are mirror images of the bottom two wafers. The actual GaAs MMIC chip is placed on the second silicon piece from the bottom. Before the two halves of the block are closed, they are shown in 5(b). Figure 6(c) shows the SEM of the vertical profile of the waveguide structure. The completed block, sandwiched between two metal waveguides is shown in Figure 6(d). The measured results indicate that the silicon package is working as well as conventional metallic waveguide blocks.

In the next step towards validating this concept we intend to design, fabricate and characterize a receiver front end with this technology. This will build on the power amplifier module shown above. The signal from the power amplifier module will be input to the tripler which in turn will pump the mixer. Both the tripler and mixer chips have been fabricated and the silicon pieces once fabricated will be used to package the submillimeter-wave components. Once each wafer has been fabricated via micro-machining and assembled with the appropriate devices we will investigate technologies to “integrate” the wafer stack.

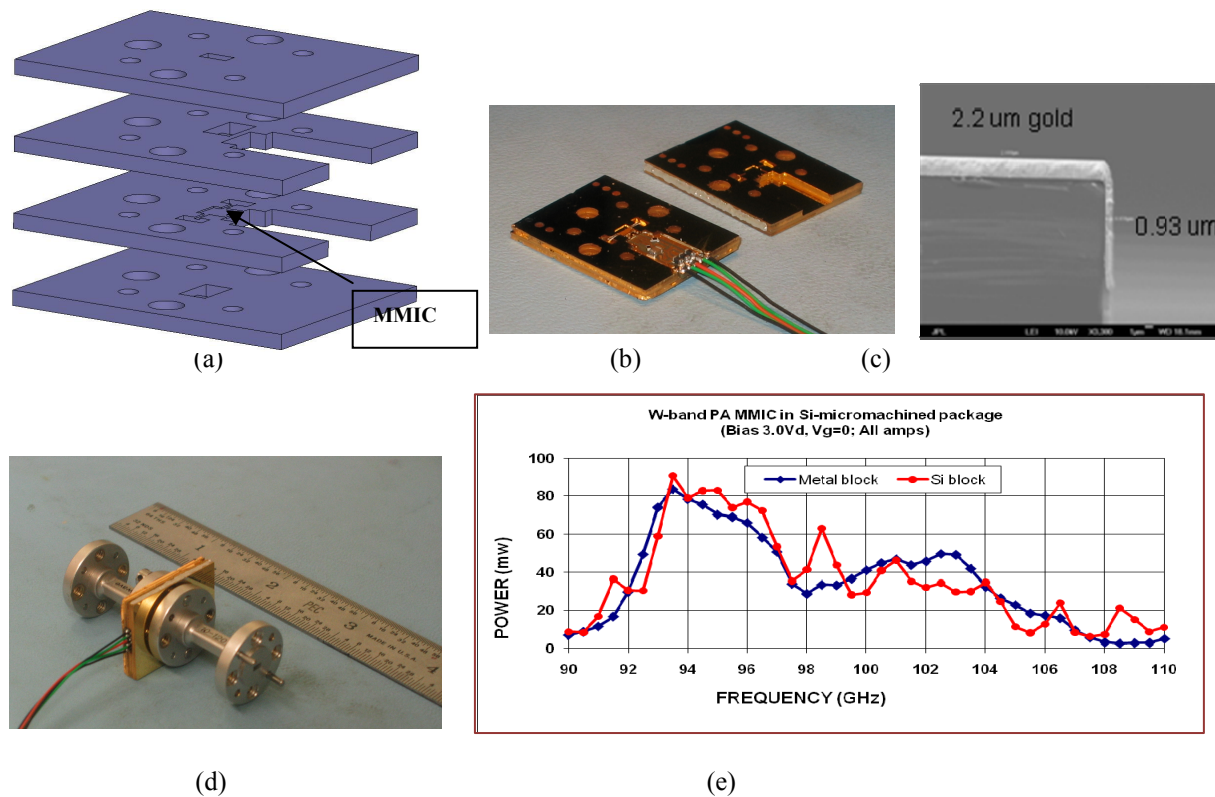


Figure 6: A GaAs power amplifier MMIC has been successfully packaged in micro-machined silicon. (a) shows the conceptual design of a 4-wafer stack for packaging a w-band MMIC power amplifier, (b) shows the MMIC chip placed in the micromachined Si wafers, (c) shows a SEM picture of the sidewall profile of a feature in silicon achieved by dry etching and gold deposition, (d) the Si package is designed with standard waveguide flange interfaces so it can be readily tested, and (e) shows a comparison of performance between a conventional metal block and the Si-micromachined block. The Si block weighs only 4 grams.

In the last few years there has been tremendous progress in bonding wafers of dissimilar material properties to take advantage of each wafer's unique capabilities [17]. A classic example of this technology is its ability to bond GaAs and Si wafers together. More recently, this concept has been validated at millimeter-wave lengths [13] demonstrating functioning W-band transmit arrays by stacking multiple wafers of GaAs to obtain dense packing factors and immense reduction in volume and power amplification functional density. We propose to expand the use of similar techniques in the submm range with the ultimate goal of producing a submm Radiometer-on-a-Chip. Finally, a concept for a 6x6 imaging array is shown in Figure 7. The W-band signal will be distributed, amplified, and tripled. A sub-harmonically pumped mixer chip will be utilized. The RF coupling will happen through the micro-lens "wafer" making for a super-compact imaging array in the 500-600 GHz range.

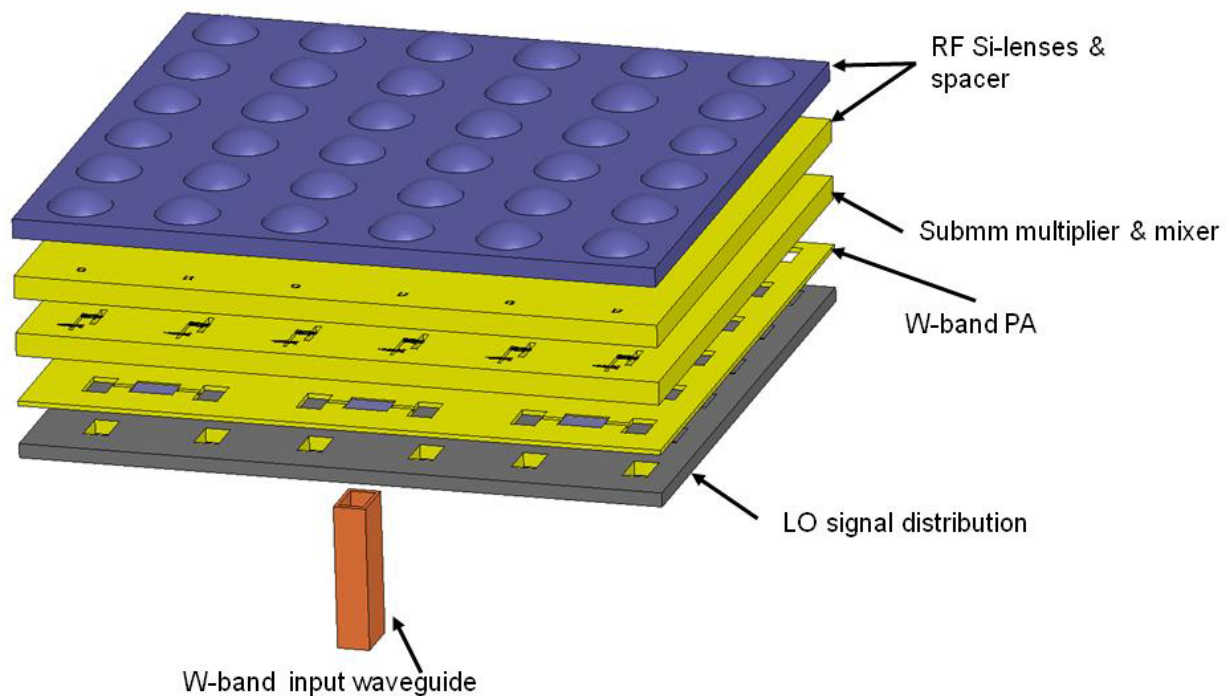


Figure 7: A proposed 6x6 array receiver for the 500-600 GHz band. The W-band signal is distributed, amplified and then tripled to drive a sub-harmonically pumped mixer. Micro-lens array is used to couple RF signal.

4. CONCLUSION

A conceptual design for a super compact submm array receiver is presented. The technique utilizes advanced semiconductor technologies such as wafer bonding and Si micro-machining to achieve receiver front ends that are low mass and low volume. A prototype W-band power amplifier module has been demonstrated and a 500-600 GHz receiver front end is under development. This technique provides the flexibility of building a radiometer-on-a-chip and opens up the possibilities of large format array receivers, multi-frequency imaging arrays, and beam-steering capability for future heterodyne array receivers.

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